Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended and new claims added to more clearly claim Applicants invention to overcome the applied art of record. No new matter has been added.

Support for the claim amendments are found in the original claims and in Specification and in the Figures e.g., Figure 2B and 4B as well as in the discussion presenting the problem to be solved and in the Specification beginning at line 18, page 17:

"For example, in a process to improve the planarity of the photoresist layer, portions of the resist layer having a relatively greater thickness, for example process wafer areas having a **relatively lower density of opening features**, for example isolated Via opening 26E in process wafer portion 27B, are selectively exposed to a **relatively higher radiant energy dosage** to produce a relatively increased dissolution rate in a subsequent developing process thereby selectively removing a relatively greater amount of resist layer 28 thickness portions to produce a resist layer with improved planarity. For example, resist layer 28 is produced having about the same thickness as the resist layer portion overlying process wafer portion 27A having a relatively lower thickness and a higher density of features, for example Via

openings 26A, 26B, 26C, 26D."

Support for new claims 28 and 30 are found in the Specification e.g., at page 7 beginning at line 14:

"For example, **if the resist thickness is within a certain thickness window, the resist removal rate will fall within a linear region e.g., area A where the resist removal rate in the development process may be adjusted linearly with an increase or decrease in radiant energy dosage.**"

Claim Rejections under 35 USC 102(b)

1. Claims 1, 2, 4-13, 15-22, and 24 stand rejected under 35 USC 102(b) as being anticipated by Sato (US 6,064,466).

Sato discloses a method for selectively exposing a resist layer over single or a plurality of semiconductor features including protrusions and trenches to form a planarized resist layer or to form resist partially filling trenches (see Abstract; col 3, lines 1-14; col 3, lines 65-67; col 4, lines 19-22; col 4, lines 45-47; col 4, lines 62-66; col 5, lines 15-18; Figures 4-7).

Sato also Sato discloses that a residual resist thickness (remaining resist following development) depends on the light intensity, the pattern density (of mask), the development time, and type of resist (col 3, lines 1-14).

Thus Sato fails to disclose several aspects of Applicants disclosed and claimed invention including:

With respect to claim 1, Sato does not disclose the following aspects of Applicants invention:

"providing a substrate comprising **a first density of semiconductor features and a second density of semiconductor features wherein said first density is greater than said second density;**"

determining a thickness of the first thickness topography;

and

"then performing an etch process to produce a third thickness topography"

With respect to claim 15, Sato does not disclose the following aspects of Applicants invention:

"providing a semiconductor wafer having a process surface comprising **a first density of via openings and a second density of via openings formed in a dielectric layer, said first density greater than said second density;**"

or

"**determining a thickness topography** of the radiation sensitive polymer layer;"

or

"selectively exposing portions of the radiation sensitive polymer layer through the exposure mask to deliver the desired radiant energy dosage **including a relatively higher radiant energy dosage to an area of said polymer layer overlying said second density**"

or

"developing the radiation sensitive polymer layer to produce the subsequent planarized thickness topography wherein said **planarized thickness topography comprises a thickness portion above and covering said vias**; and,

then performing an etchback process to form via plugs at least partially filling said vias."

Thus Sato is clearly insufficient to make out a *prima facie* case of anticipation with respect to Applicants disclosed and claimed invention.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Claim Rejections under 35 USC 103(a)

2. Claim 25 stands rejected under 35 USC 103(a) as being unpatentable over Sato, above.

Examiner admits that Sato does not disclose determining a thickness of the resist layer. Examiner argues that the thickness depends on the device produced and subsequent manufacturing steps. Examiner argues that such steps would be "within the ordinary skill".

"A statement that modifications of the prior art to meet the claimed invention would have been "`well within the ordinary skill of the art at the time the claimed invention was made'" because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a prima facie case of obviousness without some objective reason to combine the teachings of the references." *Ex parte Levengood, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993)*.

Examiner also ignores aspects of Applicants disclosure which show that the thickness of the resist layer is important (see e.g., new claims 27, 29 and 30) to achieve a desired planarization. Sato also fails to disclose Applicants claimed etchback process of a second resist layer covering semiconductor features which is important in the etchback process, but rather

teaches away therefrom, by teaching that the resist layer be made co-planar with the substrate following development or that the resist partially fills trenches following development. Nowhere does Sato suggest or disclose the application of his method in connection with a subsequent etchback process.

Thus, the disclosure of Sato does not produce Applicants disclosed and claimed invention and fails to recognize the problem that Applicants have disclosed and solved.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)*.

2. Claim 3 stands rejected under 35 USC 103(a) as being unpatentable over Sato, above, and further in view of Lewis (US 4,822,722).

Even assuming *arguendo*, a proper motivation for combination,

the fact that Lewis discloses that it is known to measure the thickness of the photoresist layer does not further help Examiner in establishing a prima facie case of obviousness.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)*.

3. Claim 14 stands rejected under 35 USC 103(a) as being unpatentable over Sato, above, and further in view of Aronsatein (US 3,889,355).

Even assuming *arguendo*, a proper motivation for combination, the fact that Aronsatein discloses various methods of resist exposure does not further help Examiner in establishing a prima facie case of obviousness.

4. Claim 23 stands rejected under 35 USC 103(a) as being unpatentable over Sato, above, and further in view of Breyer (US (US 4,333,794).

Breyer discloses a method of forming a **bipolar transistor** where a **polysilicon etchback process** is used to form portions of the emitter (see Abstract; col 10, lines 43-61; col 1, lines 1-15). Breyer discloses forming a resist plug by an etchback process to protect a 1 micron deep trench formed during etching back of an Sio2 layer (col 10, lines 43-48). Breyer discloses that the **photoresist acts as an ion implant mask** preventing ion implantation of the substrate underlying the trench with resist. (col 11, lines 16-33).

There is no apparent motivation for combining the method of Sato with the method of Breyer. For example, the etchback process of Breyer works by a different principle of operation (etched back in areas **other than the trench**) and any modification of Sato or Breyer would make either method of Sato unsuitable for its intended purpose (exposure and development vs. etchback).

Even assuming *arguendo*, a proper motivation for combination, such combination does not produce Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when

combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"The prior art must provide a motivation or reason for the worker in the art, without the benefit of appellant's specification, to make the necessary changes in the reference device." *Ex parte Chicago Rawhide Mfg. Co., 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984).*

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." *In re Ratti, 270 F.2d 810, 123, USPQ 349 (CCPA 1959).*

"If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed.*

Cir. 1984).

The Claims have been amended and new claims added to clarify Applicants' disclosed and claimed invention. A favorable reconsideration of Applicants' claims is respectfully requested.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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